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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/816,980 | 04/02/2004 | Ho-Yuan Yu | LOVO-56.DIV | 2006 |

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| EXAMINER | |
|---|---|
| BERRY, RENEE R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/816,980 | YU | |
| | Examiner | Art Unit | |
| | Renee R Berry | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) *1-10 and 21-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-10 and 21-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 and 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,707,095 to Chidambarrao in view of US Patent No. 6,576,516 to Blanchard.

In regards to claim 1, Chidambarrao teaches an electronic silicon device comprising: a silicon substrate comprising a planar surface; trench disposed in said planar surface of said silicon substrate, said trench comprising a wall and a bottom; silicon dioxide layer disposed on the bottom of said trench and also on a portion of said wall, said layer being terminated at a distance D below said planar surface of said silicon device at column 18, lines 1-16.

In regards to claim 3, Chidambarrao teaches the electronic silicon device of Claim 1, further comprising a junction field effect transistor (JFET) at column 7, lines 35-51.

In regards to claim 4, Chidambarrao teaches the electronic silicon device of Claim 1, further comprising a metal oxide semiconductor field effect transistor (MOSFET) at column 7, lines 35-51.

In regards to claim 5, Chidambarrao teaches the electronic silicon device of Claim 1, further comprising an integrated circuit at column 7, lines 35-51.

In regards to claim 6, Chidambarrao teaches the electronic silicon device of Claim 1, wherein said trench is disposed above a gate at column 18, lines 42-53.

In regards to claim 7, Chidambarrao teaches the electronic silicon device of Claim 1, wherein said trench is disposed adjacent to a source at column 18, lines 42-53.

In regards to claim 9, Chidambarrao teaches the electronic silicon device of Claim 1, wherein said silicon dioxide layer is thermally grown at column 18, lines 11-12.

In regards to claim 10, Chidambarrao teaches the electronic silicon device of Claim 1, wherein said silicon dioxide layer is deposited at column 18, lines 11-12.

In regards to claim 23, Chidambarrao the semiconductor device of Claim 21, further comprising a junction field effect transistor (JFET) at column 7, lines 35-51.

In regards to claim 24, Chidambarrao the semiconductor device of Claim 21, further comprising a metal oxide semiconductor field effect transistor (MOSFET) at column 7, lines 35-51.

In regards to claim 25, Chidambarrao the semiconductor device of Claim 21, further comprising an integrated circuit at column 7, lines 35-51.

In regards to claim 26, Chidambarrao teaches the semiconductor device of Claim 21, wherein said trench is disposed above a gate structure at column 18, lines 42-53.

In regards to claim 27, Chidambarrao teaches the semiconductor device of Claim 21, wherein said trench is disposed adjacent to a source structure at column 18, lines 42-53.

In regards to claim 29, Chidambarrao teaches the semiconductor device of Claim 21, wherein paid silicon dioxide layer is thermally grown at column 18, lines 11-12.

In regards to claim 30, Chidambarrao teaches the semiconductor device of Claim 21, wherein said silicon dioxide layer is deposited at column 18, lines 11-12.

However, Chidambarrao does not teach all the limitations of the claims.

In regards to claims 1 and 2, Blanchard teaches the electronic silicon device of Claim 1, wherein that is said polysilicon fill comprises an upper surface disposed within a distance D from said planar surface of said silicon substrate at column 9, lines 1-2.

In regards to claim 8, Blanchard teaches the electronic silicon device of Claim 1, wherein said silicon dioxide layer is between 100 angstroms and 3000 angstroms in thickness at column 4, lines 40-44.

In regards to claim 21, Blanchard teaches a semiconductor device comprising: a silicon substrate; a trench disposed in said silicon substrate, said trench comprising a wall and a bottom; a silicon dioxide layer disposed on the bottom of said trench and also on a portion of said wall, said layer being terminated below an original surface of said silicon substrate; a polysilicon fill disposed on the surface of said silicon dioxide layer and on a portion of said wall at column 8, lines 47-67

In regards to claim 22, Blanchard teaches the semiconductor device of Claim 21, wherein said polysilicon fill comprises an upper surface that is disposed between a top

surface of said silicon dioxide layer and said original surface of said silicon substrate at column 9, lines 1-2.

In regards to claim 28, Blanchard the semiconductor device of Claim 21, wherein said silicon dioxide layer is between 100 angstroms and 3000 angstroms in thickness at column 4, lines 40-44.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Chidambarrao to include a silicon substrate; a trench disposed in said silicon substrate, said trench comprising a wall and a bottom; a silicon dioxide layer disposed on the bottom of said trench and also on a portion of said wall, said layer being terminated below an original surface of said silicon substrate; a polysilicon fill disposed on the surface of said silicon dioxide layer and on a portion of said wall, since such a modification would result in substantially reduced on-resistance, as described in column 2, lines 28-31 of Blanchard.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RRB

September 26, 2004

GENE N. AUDUONG
PRIMARY EXAMINER